843.43311X00

IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A non-volatile semiconductor memory device, comprising:

a semiconductor substrate;

first and second semiconductor regions of a first conductivity type formed in said semiconductor substrate;

a first channel region and a second channel region between said first semiconductor region and said second semiconductor region in said semiconductor substrate, said first channel region being located on the side close to said first semiconductor region and said second channel region being located on the side close to said second semiconductor region;

a first gate formed above said first channel region via a first insulator; and

a second gate formed above said second channel region via a second insulator,

~~wherein writing and erasing operations are performed by injecting electric charge into said second insulator, and~~

wherein said non-volatile memory is enabled to perform at least a writing operation, an erasing operation and a charge holding operation, and such that in the writing operation electrons are injected into said second insulator, in the erasing

operation holes are injected into said second insulator and in the holding operation charges are held in said second insulator, and

wherein the charge density of an impurity in said first channel region is different from the charge density of an impurity in said second channel region.

2. (Original) The non-volatile semiconductor memory device according to claim 1,

wherein the charge density of an impurity in said second channel region is lower than the charge density of an impurity in said first channel region.

3. (Currently Amended) The non-volatile semiconductor memory device according to claim 1,

wherein ~~the~~ an impurity of a second conductivity type, opposite to said first conductivity type, is introduced into said first channel region, and the impurity of the first conductivity type and the impurity of the second conductivity type are introduced into said second channel region.

4. (Currently Amended) The non-volatile semiconductor memory device according to claim 1,

wherein said second insulator is a laminated film of a ~~10~~ silicon oxide film, a silicon nitride film, and a silicon oxide film.

5. (Original) The non-volatile semiconductor memory device according to claim 1,

wherein the thickness of said second insulator is larger than the thickness of said first insulator.

6. (Original) The non-volatile semiconductor memory device according to claim 1,

wherein the charge density of an impurity in said second channel region is set within the range of $10^{17}/cm^3$ to $10^{18}/cm^3$.

7. (Original) The non-volatile semiconductor memory device according to claim 1,

wherein said second gate is adjacent to said first gate via said second insulator.

8. (Cancel without prejudice or disclaimer)

9. (Currently Amended) A non-volatile semiconductor memory device, comprising:

a semiconductor substrate;

first and second semiconductor regions of a first conductivity type formed in said semiconductor substrate;

a first channel region and a second channel region between said first semiconductor region and said second semiconductor region in said semiconductor substrate, said first channel region being located on the side close to said first

semiconductor region and said second channel region being located on the side close to said second semiconductor region;

a first gate formed above said first channel region via a first insulator; and

a second gate formed above said second channel region via a second insulator,

~~wherein writing and erasing operations are performed by injecting electric charge into said second insulator,~~

wherein said non-volatile memory is enabled to perform at least a writing operation, an erasing operation and a charge holding operation, and such that in the writing operation electrons are injected into said second insulator and in the erasing operation holes are injected into said second insulator, in the erasing operation holes are injected into said second insulator and in the holding operation charges are held in said second insulator, and

wherein said second channel region includes a first region on the side close to said second semiconductor region and a second region on the side close to said first channel region, and the charge density of an impurity in said first region is higher than the charge density of an impurity in said second region.

10. (Currently Amended) The non-volatile semiconductor memory device according to claim 9,

wherein the impurity concentration of the second conductivity type, opposite to said first conductivity type, of said first region is higher than the impurity concentration of the second conductivity type of said second region.

11. (Currently Amended) The non-volatile semiconductor memory device according to claim 9,

wherein the impurity of the second conductivity type ~~opposite to said first conductivity type~~ is introduced into said first channel region, the impurity of the first conductivity type and the impurity of the second conductivity type are introduced into said second channel region, and the impurity concentration of the second conductivity type of said first region is higher than the impurity concentration of the second conductivity type of said second region.

12. (Original) The non-volatile semiconductor memory device according to claim 9,

wherein said second insulator is a laminated film of a silicon oxide film, a silicon nitride film, and a silicon oxide film.

13. (Original) The non-volatile semiconductor memory device according to claim 9,

wherein the charge density of an impurity in said first channel region is higher than the charge density of an impurity in said second region.

14. (Original) The non-volatile semiconductor memory device according to claim 9,

wherein said second gate is adjacent to said first gate via said second insulator.

15. – 29. (Cancelled without prejudice or disclaimer)

30. (New) The non-volatile semiconductor memory device according to claim 11,

wherein said second insulator is a laminated film of a silicon oxide film, a silicon nitride film, and a silicon oxide film.

31. (New) The non-volatile semiconductor memory device according to claim 13,

wherein said second insulator is a laminated film of a silicon oxide film, a silicon nitride film, and a silicon oxide film.

32. (New) The non-volatile semiconductor memory device according to claim 14,

wherein said second insulator is a laminated film of a silicon oxide film, a silicon nitride film, and a silicon oxide film.